IN THE SPECIFICATION:

Page 3, 5th full paragraph is herewith amended as follows:

In fulfillment of the above stated objects, and the particular need noted that has arisen in this art, the present invention, briefly stated, provides a structure comprising a system level test and burn in carrier, said structure comprising: a system for testing an array of device chips by temporarily attaching a microjoint structure, comprising a carrier, to the array, the carrier being a multilayer substrate having a plurality of receptacles provided with ~~microdendritic~~ dendritic surface features, said receptacles matching a pattern and size of microjoint pads on the device chips; test pads; interconnect wiring that connects the test pads to the ~~microdentritic~~ dendritic receptacle array, and interconnect wiring additionally providing connections between a multiplicity of the devices mounted on the carrier so as to form a complex functional system that can be adequately tested while on the carrier.

Page 4, 1st partial paragraph is herewith amended as follows:

are pushed against the ~~microdendritic~~ dendritic contacts on the carrier so as to establish a reliable temporary electrical connection for the duration and conditions of a typical test and burn in process. At the end of this regimen, any bad quality chips are removed and replaced with new chips. The regimen iteratively leads to a final collection of chips deemed to be functional at a system level with a good degree of reliability.

Page 5, 2nd full paragraph is herewith amended as follows:

It will be seen that the representative receptacle 20, as seen in Figure 1, extends into the dielectric layer 14 where contacts to the device chips are made with respect to a representative device wafer 30 with a representative stud 32 extending from it and having a metal tip ~~34~~ 39 (Figure 3). The important point to note is that the size of the receptacles 20 can be as small as about 2.5 microns. The size of the receptacle, additionally, is about 20% larger than the size of the stud 32.

Page 5, 3rd full paragraph is herewith amended as follows:

It will further be seen in Figure 1 that a liner~~/seed~~ layer 22 is deposited, which is usually constituted of 0.04 micron layers of TaN-Ta and that a seed layer 24 is constituted of ~~as well as a~~ 0.1 micron of Cu ~~layer 24~~.

Page 5, 7th full paragraph is herewith amended as follows:

Etching is now performed to remove the ~~TaN-Ta 22~~ top, planar portion of the TaN-Ta layer 22 from the region between the receptacles, the reason for doing so ~~result thereof~~ being ~~depicted in~~ understood by reference to Figure 3. Chemical or dry plasma etching can be used for this step. The finished carrier structure 10 (Figure 3) now has female receptacles 20 populated with noble metal asperities that will engage and penetrate into the softer microjoint solder or Au-Sn tipped pads ~~34~~ 39 on the device ~~chipstuds~~ chip studs 32 when the test carrier and the chip 30 are aligned and assembled together under a conformal back pressure assembly not shown in Figure 3. This contact behavior is adequate for exercising or performing system-level test and for burning in of the whole system, collectively made up of the individual chips. The tests performed under the temporary interconnection regime are not restricted to open/short-testing or to system performance test, but can include an exhaustive routine of testing to make sure the chips are good for their intended uses.